ABSTRACT OF THE DISCLOSURE

A semiconductor package and a method for forming the same are provided. The semiconductor package comprises a chip having an active surface and a back surface. The semiconductor package further comprises a substrate having an upper surface and a lower surface opposite the upper surface. The chip is electrically connected to the upper surface of the substrate. A lid is thermally coupled to the back surface of the chip. A thermal interface material (TIM) is located between the chip and the lid. The TIM includes voids to reduce thermomechanical stresses applied on the chip and the TIM, thereby preventing package cracks.